Amendments to the Specification:

Please replace the paragraph beginning at page 6, line 19, with the following rewritten paragraph:

The invention thus seeks to provide a very thin diffusion region using a known technique for growing epitaxial regions to form the very thin channel and has the advantages of providing much tighter tolerances on channel thickness than a lithographically defined channel which can be maintained by selective etching and that epitaxial growth is not complicated by ~~thee~~ the presence of thin confining layers.

Please replace the paragraph beginning at page 11, line 18, with the following rewritten paragraph:

Then, a mask is applied and positioned such that the mask opening 304, shown in Figure 3A, provides for removal of the exposed portion of silicon layer 110 and etch stop 202 within the mask opening 304. It is preferred that the mask 304 be aligned as closely as possible to the channel 204. The ~~exposedd~~ exposed silicon 110 within mask opening 304 is then etched using an anisotropic etch.

Please replace the paragraph beginning at page 13, line 14, with the following rewritten paragraph:

Figure 8A is a representational cross-sectional cut of section 1-1 of Figure 11B. Figure 8A is representational because polysilicon conductor (PC) resist 802 and STI fill 702 are present during fabrication in Figure 8A, but are not present in

corresponding region ~~141~~ 114 of Figure 11B. After placing the PC resist mask 802 on a selected regions of STI fill 702, STI fill 702 is selectively etched relative to pad films 104 and down to the BOX layer 108. It is preferred, but not required, that the etch also be selective relative to the BOX layer 108. Pad films 104 are then removed selectively to the STI fill layer 702 and BOX layer 104. Figures 9A and 10A show that the pad layers 104 could be left, if desired, to allow a thin gate dielectric 904 only on the sidewalls of channels 204, 502 and 602. It is preferred that there be approximately a 10:1 selectivity in each etch, which can be accomplished with known state of the art etches. If desired, well implants may optionally be introduced at this point. These implants would be done using highly angled implants, preferably in the range of 10 to 45 degrees, with each implant rotated at approximately 90 degrees relative to each other in order to fully dope the sidewalls of the diffusion. In order to avoid doping the surface layer of the diffusions more heavily than the sides, the implantation could be done before removing the pad films 104 in the exposed areas of PC resist 802.

Please replace the paragraph beginning at page 14, line 11, with the following rewritten paragraph:

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Figure 9A shows the substrate of Figure 8A after gate dielectric growth 904 (e.g., SiO_2), and gate conductor 902 deposition. It should be understood that nitrided oxides, nitride/oxide composites, metal oxides (e.g., Al_2O_3, $ZrSiO_4$, TiO_2, Ta_2O_5, ZrO_2, etc.), perovskites (e.g., (Ba, Sr)TiO_3, La_2O_3) and combinations of the above can also be used as the dielectric. Gate dielectric growth on each channel 204, 502 and 602 could be standard furnace or single-wafer chamber oxidations in accordance with conventional methods. If desired, nitriding species (e.g., N_2O, NO or N_2 implantation)

can be introduced prior to, during, or subsequent to oxidation. Gate dielectric deposition on each channel 204, 502 and 602 can be ~~can be~~ accomplished, for example, through chemical vapor deposition (CVD) or other techniques known to those skilled in the art.